IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently Amended) An integrated circuit structure comprising:

a substrate having at least two types of crystalline orientations;

first-type transistors formed on first portions of said substrate having a first type of crystalline orientation;

second-type transistors formed on second portions of said substrate having a second type of crystalline orientation; and

a straining layer above said first-type transistors and said second-type transistors,

wherein said first portions of said substrate comprise a first layer at a top of said first portions, said first layer having said first type of crystalline orientation and a second layer at a bottom of said first portions, said second layer having said second type of crystalline orientation, and

wherein said second portions of said substrate comprise said second layer at a bottom of said second portions and a third layer at a top of said second portions, said third layer having said second type of crystalline orientation and said third layer contacting said second layer ~~and are devoid of said layer having said first type of crystalline orientation~~.

2. (Original) The structure in claim 1, wherein said first-type transistors and said second-type transistors include silicide regions and said straining layer is above said silicide regions.

3. (Previously Presented) The structure in claim 2, wherein each of said first-type transistors and said second-type transistors include source and drain regions formed within said substrate and a gate conductor formed over said substrate between said source and drain regions, and

wherein said silicide regions are formed over said gate conductor and said source and drain regions.

4. (Original) The structure in claim 1, wherein said first-type transistors are

complementary to said second-type transistors.

5. (Original) The structure in claim 1, wherein said first portions of said substrate comprise non-floating substrate portions and said second portions of said substrate comprise floating substrate portions.

6. (Canceled).

7. (Original) The structure in claim 1, wherein said first-type transistors and said second-type transistors comprise one of planar complementary metal oxide semiconductor (CMOS) transistors and fin-type field effect transistors (FinFETs).

8. (Currently Amended) An integrated circuit structure comprising:

a substrate having at least two types of crystalline orientations;

N-type field effect transistors (NFETs) formed on first portions of said substrate having a first type of crystalline orientation;

P-type field effect transistors (PFETs) formed on second portions of said substrate having a second type of crystalline orientation; and

a straining layer above said NFETs and said PFETs,

wherein one of said first portions and said second portions of said substrate comprise a first layer at a top, said first layer having said first type of crystalline orientation and a second layer at a bottom, said second layer having said second type of crystalline orientation, and

wherein the other of said first portions and said second portions of said substrate comprise said second layer at a bottom and a third layer at a top, said third layer having said second type of crystalline orientation and said third layer contacting said second layer ~~a layer having one of said first type of crystalline orientation and said second type of crystalline orientation and are devoid of a layer having the other of said first type of crystalline orientation and said second type of crystalline orientation~~.

9. (Original) The structure in claim 8, wherein said NFETs and said PFETs include silicide regions and said straining layer is above said silicide regions.

10. (Previously Amended) The structure in claim 9, wherein each of said NFETs and said PFETs include source and drain regions formed within said substrate and a gate conductor formed over said substrate between said source and drain regions, and

wherein said silicide regions are formed over said gate conductor and said source and drain regions.

11. (Original) The structure in claim 8, wherein said NFETs are complementary to said PFETs.

12. (Original) The structure in claim 8, wherein said first portions of said substrate comprise non-floating substrate portions and said second portions of said substrate comprise floating substrate portions.

13. (Canceled).

14. (Original) The structure in claim 8, wherein said NFETs and said PFETs comprise one of planar complementary metal oxide semiconductor (CMOS) transistors and fin-type field effect transistors (FinFETs).

15-20. (Canceled).

21. (Previously Presented) The structure in claim 1, further comprising an insulator layer separating said layer having said first type of crystalline orientation from said layer having said second type of crystalline orientation.

22. (Previously Presented) The structure in claim 8, further comprising an insulator layer separating said layer having said first type of crystalline orientation from said layer having said second type of crystalline orientation.

23. (Currently Amended) An integrated circuit structure comprising:

a substrate having at least two types of crystalline orientations;

first-type transistors formed on first portions of said substrate having a first type of crystalline orientation,

second-type transistors formed on second portions of said substrate having a second type of crystalline orientation; and

wherein said first portions of said substrate comprise a first layer at a top of said first portions, said first layer having said first type of crystalline orientation and a second layer at a bottom of said first portions, said second layer having said second type of crystalline orientation, and

wherein said second portions of said substrate comprise said second layer at a bottom of said second portions and a third layer at a top of said second portions, said third layer having said second type of crystalline orientation and said third layer contacting said second layer ~~and are devoid of said layer having said first type of crystalline orientation~~.

24. (Previously Presented) The structure in claim 23, further comprising an insulator layer separating said layer having said first type of crystalline orientation from said layer having said second type of crystalline orientation.

25. (Previously Presented) The structure in claim 23, wherein said first-type transistors and said second-type transistors include silicide regions.

26. (Previously Presented) The structure in claim 25, wherein each of said first-type transistors and said second-type transistors include source and drain regions formed within said substrate and a gate conductor formed over said substrate between said source and drain regions, and

wherein said silicide regions are formed over said gate conductor and said source and drain regions.

27. (Previously Presented) The structure in claim 23, wherein said first-type transistors are complementary to said second-type transistors.

28. (Previously Presented) The structure in claim 23, wherein said first portions of said substrate comprise non-floating substrate portions and said second portions of said substrate comprise floating substrate portions.